REMARKS

Claims 1-20 are pending. Applicants respectfully traverse, request reconsideration and withdrawal of the rejections for the following reasons.

I. Summary of the Examiner's Objections/Rejections

Claims 1-10 and 12-19 are rejected under 35 U.S.C. §103(a) over U.S. Patent Number 6,446,193 to Alidina et al. ("*Alidina*"), in view of U.S. Patent No. 5,896,517 to Wilson. Claims 11 and 20 are rejected under 35 U.S.C. §103(a) over *Alidina*, in view of *Wilson* and in further view of U.S. Patent Number 5,673,377 to Berkaloff. Claim 16 is objected to due to an informality.

II. Applicant's Response to the Examiner's Rejections

The Applicants traverse the aforementioned claim rejections for at least the reasons set forth in greater detail below.

A. Objection to Claim 16.

The Applicants' attorney thanks the Examiner for the suggestion; however, the replacement language appears identical to the language to replace. A clarification is requested.

B. 35 U.S.C. §103(a); Claims 1-10 and 12-19.

According to the Office Action, claims 1-10 and 12-19 are rejected under 35 U.S.C. §103(a) over U.S. Patent Number 6,446,193 to *Alidina* et al. ("*Alidina*"), in view of U.S. Patent No. 5,896,517 to *Wilson*.

Alidina is directed to reducing instruction cycles in a digital signal processor by processing two different register parts in a single processor cycle instead of two. (*Alidina*, Col. 2, lines 42-56). The Office Action acknowledges that *Alidina* does not teach multi-threading and having registers and operands that correspond to each individual thread.

Wilson is directed to a method for improving the performance of a computer system by performing useful work in parallel with long-latency main memory accesses. (*Wilson* ¶3, lines 14-21, ¶3, lines 4-8). Instructions are added at the program writing stage by the programmer, or by software tools such as a compiler, to pre-fetch data from main memory in order to avoid the overhead of multi-threaded process swapping because of blocking, such as a cache miss. (*Wilson*, Col. 3, lines 14-28). The overhead of multi-threaded process swapping (such as needing data from a disk due to a cache miss) can be quite expensive since there may be many registers to save and restore. (*Wilson*, Col. 2, lines 34-65). Because of the high overhead costs, and because such process-swapping is always unexpected, "It is desirable to avoid the overhead costs of process-swapping," i.e., the multi-threaded processor scheme. (*Wilson*, Col. 2, line 66- Col. 3 line 3).

NEITHER *ALIDINA* NOR *WILSON* TEACHES AT LEAST "WHEREIN A SELECTED ACCUMULATION REGISTER THAT CORRESPONDS TO THE SELECTED THREAD STORES THE FIRST OPERATION RESULT CORRESPONDING TO THE SELECTED THREAD"

The Office Action fails to establish a *prima facie* case of obviousness because the Office Action fails to show how each and every element in the claims is taught by the references. To establish a *prima facie* case of obviousness, each and every element arranged, as required by the claims, must be taught or suggested in the prior art. MPEP 2143.03.

According to the Office Action dated 8/27/03, ¶35, the "lines relied upon in *Wilson*'s disclosure are in the Background of the Invention, which teaches generally accepted knowledge about multi-threading and how multi-threading generally operates, and these lines did not include anything dealing with the invention of *Wilson* nor its objectives." Contrary to this assertion, *Wilson* in the Summary of the invention explicitly describes a preferred embodiment of the present of the invention as avoiding the overhead of process-swapping. (*Wilson* ¶3, lines 25-

28). *Wilson* describes a method and mechanism by which the program can specify prefetching of data to a quickly accessible data cache, and by which the program can determine which such prefetches have completed. (*Wilson*, ¶3, lines 14-25). This mechanism makes it possible to improve the performance of the computer system through the effective use of added concurrency while avoiding the overhead of process-swapping. (*Wilson*, ¶3, lines 25-28. . ., emphasis added). Consequently, *Wilson* explicitly avoids process-swapping with respect to the objects in a preferred embodiment of the present invention. With respect to the Background of the Invention, *Wilson* explicitly states "it is the primary object of the present invention . . . to do useful work in parallel with long latency main memory accesses." (*Wilson*, ¶3, lines 4-5). Therefore, the assertion in the Office Action in ¶35, the "lines relied upon" in the Background of the Invention did not include anything dealing with the invention of *Wilson* nor its objectives is contradicted by the explicit teachings of *Wilson* at Column 3, lines 4-8.

The Office Action acknowledges that *Alidina* does not teach, "wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread." Further, *Alidina* is directed to processing two different register parts in a single processor cycle for speech coding and, as a result, is directed to a problem different than the claims (*Alidina*, Col. 2, lines 42-56). *Wilson* fails to teach, among other things, a multi-threaded system as claimed. *Wilson* instead teaches, "it is desirable to avoid the overhead costs of processing swapping," i.e., multi-threaded context switching, because multi-threaded switching can be quite expensive since there may be many registers to save and restore. (*Wilson*, Col. 3, lines 26-29). Secondly, *Wilson*, as cited, fails to teach "wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread" because, in contrast to the claims, *Wilson* teaches

away from multi-threaded processing. *Id.* Further, *Wilson* teaches away from storing a thread in an accumulation register because *Wilson* teaches "multi-threaded context switching can be quite expensive since there may be many registers to save and restore." Therefore, the combination of *Alidina* in view of *Wilson*, as cited, fails to teach "wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread" as arranged in the claims. Consequently, the Office Action fails to establish a *prima facie* case of obviousness.

There is no motivation to combine *Alidina* with *Wilson* because *Wilson* teaches against the claims since, as previously stated, *Wilson* teaches avoiding multi-threaded context switching to avoid the expense of "many registers to save and restore." (*Wilson*, Col. 2, line 66 - Col. 3, line 3).[1] The very portion of *Wilson* cited in the Office Action to provide motivation to combine *Alidina* with the teachings of *Wilson* actually teaches against the claims. As previously stated, *Wilson* teaches "with a multi-threaded processor, context switching can be quite expensive since there may be many registers to save and restore" and, therefore, multi-threaded processing is avoided. As a result, there is no motivation to combine the references since *Wilson* teaches against the claims. Consequently, the Office Action fails to establish a *prima facie* case of obviousness.

Fourthly, to the extent *Alidina* and *Wilson* may be combined, such a combination would teach reducing instruction cycles in a digital signal processor by processing two different register parts in a single processor cycle, instead of two, by adding instructions at the program writing stage, by the programmer or by software tools, such as a compiler, to prefetch data from main memory in order to avoid the overhead of multi-threaded process swapping. As a result, the

combination of *Alidina* and *Wilson* is directed to a different problem than the claims. Therefore, the combination of *Alidina* in view of *Wilson*, as cited, teaches away from the claims and fails to teach each and every element as arranged in the claims. Consequently, the Office Action fails to establish a *prima facie* case of obviousness.

THE MODIFICATION OF *ALIDINA*, AS SUGGESTED BY *WILSON*, WOULD CHANGE THE PRINCIPLE OF OPERATION OF THE CLAIMED INVENTION, AND THEREFORE THE OFFICE ACTION FAILS TO PROVIDE ANY MOTIVATION TO COMBINE THE REFERENCES

The modification of *Alidina*, in view of the cited suggestion of *Wilson*, would change the principle of operation of the claimed invention because the modification suggested by *Wilson*, as previously stated, rather than teaching multi-threaded context switching, teaches "it is desirable to avoid the overhead costs of process-swapping." Instead of multi-threaded processing as claimed, *Wilson* teaches coding at the program writing stage to prefetch data. Further, the proposed combination teaches multi-threaded context switching can be quite expensive, since there may be many registers to save and restore. Therefore, the modification suggested by *Wilson* would change the principle of operation of the claimed invention because *Wilson* (1) teaches coding at the program writing stage to prefetch data, (2) teaches against multi-threaded context switching, and (3) teaches against saving and restoring registers.[2] Consequently, for at least these reasons, there is no motivation to combine the references and, therefore, the Office Action fails to establish a *prima facie* case of obviousness.

---

[1] A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. (*W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984) MPEP 2141.02).

[2] If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959). See MPEP 2143.01.

NEITHER *ALIDINA* NOR *WILSON* TEACHES AT LEAST "A SELECTION BLOCK OPERABLY COUPLED TO THE PLURALITY OF ACCUMULATION REGISTERS AND THE FIRST OPERATION UNIT, WHEREIN THE SELECTION BLOCK SELECTS THE SECOND OPERAND PROVIDED TO THE FIRST OPERATION UNIT FROM A SET OF POTENTIAL OPERANDS, WHEREIN THE SET OF POTENTIAL OPERANDS INCLUDES CONTENTS OF EACH ACCUMULATION REGISTER OF THE PLURALITY OF ACCUMULATION REGISTERS"

According to the Office Action, there is a path from the control registers via the SMUX to the first operation unit. However, the Office Action fails to show which of the many blocks in Fig. 3 function as a first operation unit, and therefore, the Applicant requests that the Examiner show which block is the first operation unit. Nevertheless, the path, as asserted, passes through other blocks, and therefore some teaching must be shown for routing the signal through the many blocks in order to form the path. Firstly, the Office Action simply states that there is a path, but fails to describe the path and the required routing. Fig. 3 fails to show the specific routing path, and further fails to show the required control signals to establish any such path, as asserted in the Office Action.

Fig. 3 teaches performing arithmetic functions rather than a multi-thread process, and therefore solves a different problem than the instant application. Consequently, the extra functional blocks for performing the arithmetic functions beyond those needed for performing process swapping in the multi-thread environment would add unnecessary expense and complexity, and would hinder performance in a multi-thread environment because of the unnecessary hardware and processing. Accordingly, the complex arithmetic unit taught by *Alidina* actually teaches away from the claimed invention because the added complexity and the resultant reduction of speed and performance would not be suitable for performing process swapping in a multi-thread environment. Furthermore, modifying the arithmetic logic unit in *Alidina*, as suggested in the Office Action, to perform process swapping in a multi-thread environment, would require elimination of the arithmetic functions, thus rendering *Alidina*

unsatisfactory for its intended purpose as an arithmetic unit, since the arithmetic unit would need to be removed to achieve the performance requirements for process swapping.[3]

Furthermore, the combination of *Alidina* and *Wilson* fail to teach "a selection block operably coupled to the plurality of accumulation registers and the first operation unit, wherein the selection block selects the second operand provided to the first operation unit from a set of potential operands, wherein the set of potential operands includes contents of each accumulation register of the plurality of accumulation registers." (*Alidina*, Col. 4, lines 57-59).

The Office Action asserts that the SMUX, as cited in *Alidina*, is the claimed selection block. However, as shown above, *Alidina* does not teach a path from the control registers via the SMUX to the first operation unit (no equivalent element in *Alidina* identified in the Office Action), but rather the XYFB couples SMUX to the register X(32). In *Alidina*, "the eight accumulators are controlled according to modes defined by preselected mode bits provided by control registers auc0 and auc1 to selectively provide feedback along a feedback path XYFBK to the x-y multiplier registers x(32) and y(32)." (*Alidina* Col 5. lines 13-17). If the rejection is maintained, and the registers x(32) in *Alidina* are equated to the first operation unit rather than the accumulation registers, then *Alidina* fails to teach at least "wherein the operation unit combines the first and second operands to produce a first operation result corresponding to the selected thread," as claimed. Therefore, *Alidina* does not teach "wherein the selection block selects the second operand provided to the first operation unit from a set of potential operands, wherein the set of potential operands includes contents of each accumulation register of the plurality of accumulation registers." Therefore, the combination of *Alidina*, in view of *Wilson*,

[3] If the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 200, 221 USPQ 1125 (Fed. Cir. 1984), MPEP 2143.02.

as cited, fails to teach each and every element as arranged in the claims. Consequently, the Office Action fails to establish a *prima facie* case of obviousness.

NEITHER *ALIDINA* NOR *WILSON* TEACHES AT LEAST "A FIRST OPERATION UNIT OPERABLY COUPLED TO RECEIVE A FIRST OPERAND AND A SECOND OPERAND CORRESPONDING TO AN OPERATION CODE ISSUED BY A SELECTED THREAD OF THE PLURALITY OF THREADS, WHEREIN THE OPERATION UNIT COMBINES THE FIRST AND SECOND OPERANDS TO PRODUCE A FIRST OPERATION RESULT CORRESPONDING TO THE SELECTED THREAD"

The Office Action cites *Alidina* (*Alidina*, Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3) for teaching "a first operation unit operably coupled to receive a first operand and a second operand corresponding to an operation code issued by a selected thread of the plurality of threads." However, as stated in the previous response, this general reference to over 70 lines in a reference without showing equivalent claim elements does not make apparent nor explain with specificity how each claim is rejected. MPEP 706, CFR 1.104(c)(2). For example, Applicants are unable to find any reference in *Alidina*, as cited, "corresponding to an operation code issued by a selected thread of the plurality of threads," as claimed. As previously stated, Applicants cannot find where *Alidina* teaches multi-threaded processing. Further, as previously stated, *Wilson* teaches against a multi-threaded processor since *Wilson* teaches "it is desirable to avoid the overhead costs of processing swapping," and multi-threaded context switching can be quite expensive, since there may be many registers to save and restore. Consequently, among other things, the combination of *Alidina*, in view of *Wilson*, as cited, fails to teach "a first operation unit operably coupled to receive a first operand and a second operand corresponding to an operation code issued by a selected thread of the plurality of threads." Therefore, the combination of *Alidina* in view of *Wilson*, as cited, fails to teach each and every element as arranged in the claims. Consequently, the Office Action fails to establish a *prima facie* case of obviousness.

The Office Action fails to indicate and Applicants are unable to find any reference to where *Alidina* or *Wilson*, as cited, teaches "wherein the operation unit combines the first and second operands to produce a first operation result corresponding to the selected thread." The Office Action acknowledges that *Alidina* fails to teach "wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread." As previously stated, *Wilson* teaches against multi-thread processing. Consequently, the combination of *Alidina* and *Wilson* teaches against "wherein the operation unit combines the first and second operands to produce a first operation result corresponding to the selected thread." If the Examiner maintains this rejection, Applicants again respectfully request a showing in *Alidina* and *Wilson* of each and every element arranged as claimed.

C. 35 U.S.C. §103(a); Claims 11 and 20.

Claims 11 and 20 are rejected under 35 U.S.C. §103(a) over *Alidina* in view of *Wilson*, and, in further view, of U.S. Patent Number 5,673,377 to Berkaloff. The Office Action acknowledges that *Alidina* does not teach multi-threading and having registers and operands which correspond to each individual thread. The Office Action acknowledges that *Alidina* does not teach wherein the first register section accumulates diffuse color information corresponding to graphics primitives, and wherein the second register section accumulates specular color information corresponding to the graphics and primitives. Further, the motivation provided in the Office Action to combine the references, "because it is needed in the calculations to create effective images," provides no basis for the meaning of "effective images," and further uses circular reasoning, and therefore fails to establish motivation to combine the references. Claims 11 and 20 add additional novel and nonobvious subject matter, and are also allowable at least for the above reasons, and as depending from an allowable base claim.

As to claim 2, the Office Action cites *Alidina* as teaching a control block as claimed. However, this portion describes bus-accessible control registers rather than "a control block operably coupled to the selection block and the plurality of accumulation registers, wherein the control block receives information based on the operation code and generates control information provided to the plurality of accumulation registers and the selection block, wherein the control information provided to the plurality of accumulation registers causes the selected accumulation register to store the result corresponding to the selected thread when the operation code corresponds to an accumulate operation." The Office Action fails to show how *Alidina* teaches that the bus-accessible control registers are equivalent to the control block as claimed and, therefore, fails to establish a *prima facie* case of obviousness. Applicants at least reassert that the references do not teach each and every element, as arranged in the claims with respect to claim 1. Claim 2 adds additional novel and nonobvious subject matter for at least these reasons, and is also allowable, at least, as depending from an allowable base claim.

As to claims 3, 4, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 18, and 19, Applicants at least reassert the above reasons. Each claim adds additional novel and nonobvious subject matter and is at least as depending from an allowable base claim. Further, the combined references do not teach each and every element as arranged in the claims.

As to claims 7 and 17, the cited portion of *Wilson*, rather than teaching an arbitration module, as asserted in the Office Action, teaches against arbitration in a multi-threaded processor since *Wilson* teaches against multi-threaded processing, as previously stated. Accordingly, the assertion that it is inherent, and that there must be a unit as claimed, is improper. A supporting reference is respectfully requested if the rejection is maintained. The Office Action acknowledges that *Alidina* does not teach multi-threading and having registers and operands that

correspond to each individual thread. Further, the Office Action on p.12, ¶26 acknowledges that *Alidina* fails to teach an arbitration module that receives command codes corresponding to a plurality of threads, wherein at least a portion of the command codes corresponding to a plurality of threads, wherein at least a portion of the command codes correspond to multiply and accumulate operations, wherein the arbitration module determines an order of execution of the command codes. Applicants also at least reassert the above statements *inter alia*, and that the references do not teach each and every element as arranged in the claims with respect to claim 1. Claims 7 and 17 add additional novel and nonobvious subject matter, and are also allowable at least as depending from an allowable base claim.

Applicant respectfully submits that the claims are in condition for allowance, and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: ~~October 31, 2003~~

By _____ NOV 19, 2003
Themi Anagnos, Reg. No. 47,388

Vedder, Price, Kaufman & Kammholz, P.C.
222 North LaSalle Street
Chicago, Illinois 60601
PHONE: (312) 609-7970
FAX: (312) 609-5005